Claims

What is claimed is:

1. A process for controlling a memory component, comprising the steps:
- Sending out a signal to select one of several possible modes for the memory component; and
- Operating the memory component in accordance with the specific mode selected by the signal.

2. The process of claim 1, additionally comprising the step:
- Writing of data into the memory component in accordance with the specific mode selected by the signal.

3. The process of claim 2, whereby one of the possible modes is a soft writing mode.

4. The process of claim 2, whereby one of the possible modes is a non-volatile writing mode.

5. The process of claim 2, whereby one of the possible modes is a hard writing mode.

6. The process of claim 2, whereby for the writing of data into the memory component - depending on the selected mode - the current intensity and/or the duration of a programming pulse is adapted, and/or the number of programming pulses.

7. The process of claim 1, whereby the memory component comprises PMC memory cells.

8. The process of claim 1, whereby the signal is sent out over one or several separate mode selection lines.

9. The process of claim 1, whereby the signal is sent out over the same line as actual data to be stored in the memory component.

10. The process of claim 9, whereby the signal is sent out over said line by use of memory mode selection bits, said bits being followed by bits carrying the data to be stored in the memory component.

11. A memory system, comprising:
- a memory component, and
- a controller, the controller being adapted to operate the memory component in one of several possible modes.

12. The system of claim 11, whereby one of the possible modes is a soft writing mode.

13. The system of claim 11, whereby one of the possible modes is a non-volatile writing mode.

14. The system of claim 11, whereby one of the possible modes is a hard writing mode.

15. The system of claim 11, whereby the memory component comprises PMC memory cells.